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Beyond Moore's Law: A co-design computing alternative.

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Beyond Moore's Law: The Nano-Scale Computing Alternative

Moore's Law was formulated by Gordon Moore of INTEL in the mid-1960s as a result of his observation on the consistency of microprocessor production trends at that time (Stallings, 1996). The *Law* supports the trend of doubling transistor density approximately every 18 months. Over the course of nearly four decades, Moore's Law has continued to hold true (Figure 1). The *Law* is, however, not truly a law. It is only a characterization of a trend that has held true for some period of time. Though we have come accustomed to accepting it as a truth, there are undeniable reasons why Moore's Law cannot continue to endure beyond the next decade or so with continued reliance on the technologies it has as its foundation – complementary metal-oxide semiconductor (CMOS). It is the purpose of this essay to illuminate how CMOS is contributing to the collapse of Moore's Law and to present an argument supporting focused research on a recommended solution that may allow for the *Law* to hold true for decades to come.

The Demise of Moore's Law

It is logical to deduce that Moore's Law is bounded by the laws of physics. The Law is concerned with density – specifically, the number of transistor per unit of area. Through reduction in the size of the transistors and lessening the space between them, it has been possible to continue this theme of miniaturization with astonishing success. It is projected that continued this trend will yield $3x10^9$ transistors per cm^2 by the year 2016 (Butts, DeHon, & Goldstein, 2002) though this is anticipated to be very near the theoretical limit of CMOS fabrication process that utilizes optical lithography (Lerner, 1999). This is due in part to the frequency of the beams being used to etch the chips as well as amount of research investment required to build the

exposure equipment, resist materials, mask technology, and metrology improvements (Wauters, 1998).

CMOS/Nano Co-Design

In confronting Moore's Law as it nears its anticipated terminal limits, our CMOS dominated semiconductor fabrication industry must synthesize a strategy for continued viability into the next era of computing. Research has been ongoing for decades in search of the technologies with the greatest promise and some success has resulted. Quantum computing (Bernstein, 2003; Bullock & Markov, 2003; Shor, 1998) has tremendous potential, though it will likely remain in the theoretical realm for decades to come with only limited demonstrations performed under tightly controlled environments. While the promise of Quantum Computing is truly impressive, the excessive time horizon until implementation exempts it from consideration as a direct follow-on to CMOS-based computing. Biologically-based computing (e.g. DNA or cellular computing) is somewhat less ambition and may result in assemblages of systems within the next few decades (Abelson et al., 2000). Again, this is too futuristic to be considered for relief from the faltering Moore's Law.

A line of research with significant promise and a shorter time horizon until implementation is characterized by the name *NanoFabrics*. The following paragraphs provide a brief overview of this technology, its fundamental principles, proposed fabrication techniques, and targeted applications.

Technology Overview

Goldstein and Budiu (2001) proposed the notion of the NanoFabric as an architectural construct "designed to overcome the constraints associated with directed assembly of nanometer-

scale components and exploit the advantages of molecular electronics" (p. 180). The fabric (Figure 2) is formed from *nanoBlocks* that are logic blocks used to perform Boolean functions and can also be used as switches to route signals.

The fabrication process envisioned for the construction of NanoFabric is anticipated to be far more cost effective than the lithographic processes of today. Such efficiencies must be realized to allow the solution to be economically feasible. Much of the costs of today's processes are the result of meticulous design prior to fabrication and extensive testing (e.g. defect detection) after fabrication. It is anticipated that such rigor will not be possible for components at the nano-scale. The alternative is to allow for significant numbers of defects within the design and fabrication phases and to execute routines on the constructed device that will identify defects and effectively isolate them during a subsequent configuration phase (Butts, DeHon & Goldstein, 2002). Such an approach is in marked contrasts to the CMOS chips of today that are generally hard-wired during fabrication. Such an approach reflects a defect-tolerant perspective rather than the defect-avoidance perspective of today.

Fabrication Techniques

The NanoFabric architecture avoids the costs and complexity of design that has been anticipated in nano-scale devices. It expects to accomplish this by applying chemically assembled electronic nanotechnology (CEAN) as a bottom-up fabrication strategy. Goldstein and Budiu (2001) assert that, like NanoFabric, many other nano-scale devices "must be created and connected through self-assembly and self-alignment instead of lithography" (p. 179).

Zeigler and Stan (2002) point out that while employing a bottom-up approach allows for manipulation at the atomic and molecular scale, it is limited in that it cannot create the complex structures produced through modern lithography. Such a limitation is not in itself prohibitive.

Research by multiple teams (Becket, 2003; Butts, DeHon & Goldstein, 2002; Goldstein & Budiu, 2001; Zeigler and Stan, 2002) have proposed the architectures that marry nano-scale technologies such as NanoFabric together with conventional CMOS structures (Figure 3). Such a strategy may leverage well understood lithographic fabrication processes to provide power, clock lines, I/O interfaces, and support logic for the NanoFabric and employ the nanotechnology to provide logic and routing switches. Such a strategy expands the utility of the technology and minimizes the challenges of bringing it to market. Justifications for this assertion are provided in the following paragraph.

Targeted Applications

The efficiency of software developers is in large part due to the multiple levels of abstraction that are used to conceal the detailed implementation of the hardware. As those levels of abstraction are removed, it is arguable that the rigor needed to manipulate the hardware increases as does the cost as a measure of development and testing time. If it is possible maintain the abstracted view visible to a developer while altering the underlying hardware, there should be no impact to the efficiency realized. This line of reasoning is evident in the assertion made by Gergel, Craft, & Lach (2003) that “traditional abstraction-based design methodology will help make the transition to nano-based design as transparent to circuit designers and tools as possible” (p. 63). One may reasonably surmise that success will be more probable for the enterprise that focuses on creating levels of abstraction for the nanotechnologies than those who endeavor to create novel interface strategy as new technologies emerge.

Conclusions

Butts et al. assert that by the year 2010 each designer will be able to design as many as 3300 gates per day. Producing designs of a billion gates will require 1200 design-work-years to complete. Beckett (2003) emphasizes the reduction in cost and greater yields resulting form nano-scale fabrication that provide for reconfigurability. This is based on the tolerance of such constructs to fabrication defects that can be configured around after fabrication. The available research suggests that pursuing a CMOS/NanoFabric co-design strategy may result in a greater probability of successfully transitioning to the post-CMOS-centric computing era.

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Figure 1

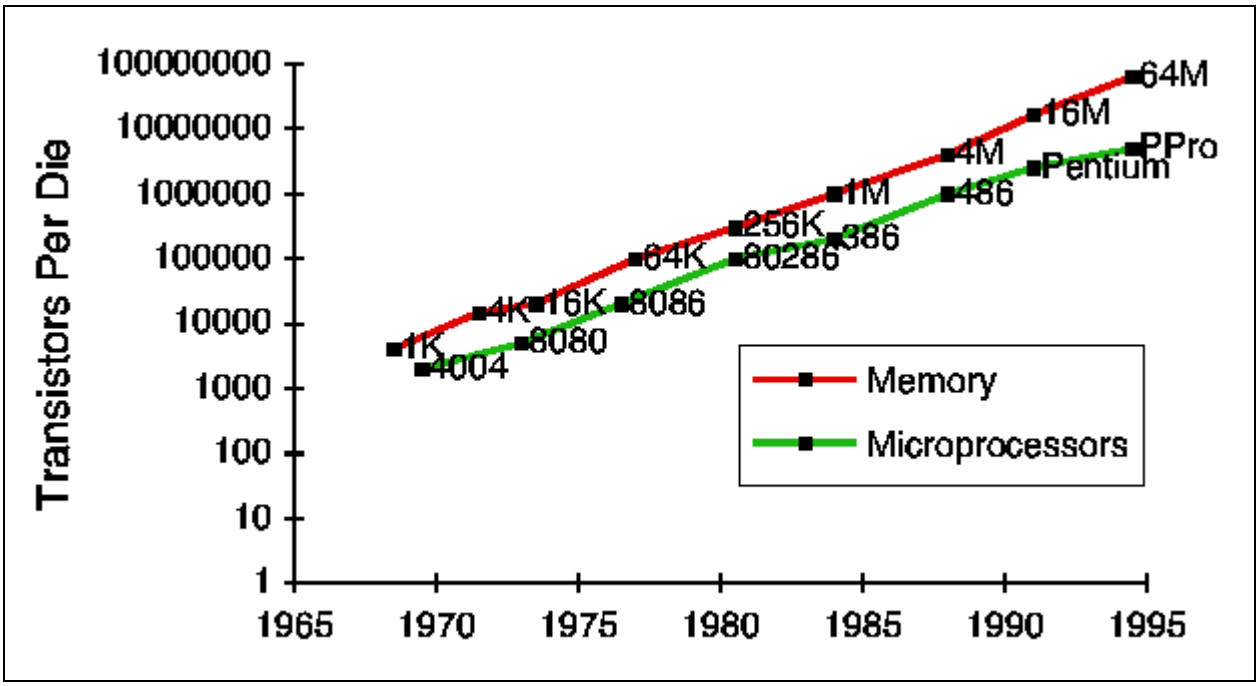

Figure 1. Transistor capacity growth over time. (Lazowska, 1996)

Figure 2

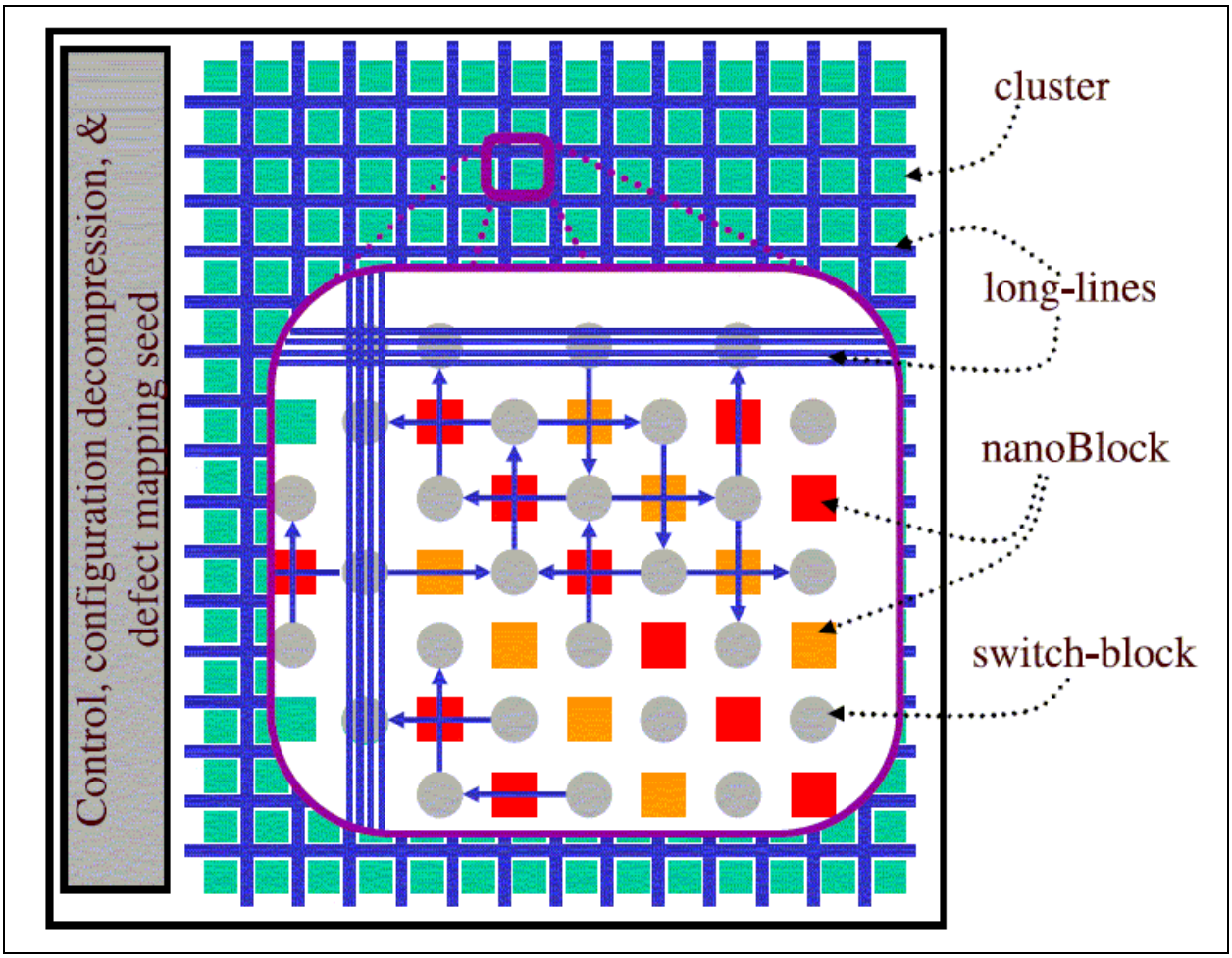

Figure 2. NanoFabric layout. (Butts, DeHon & Goldstein, 2002)

Figure 3

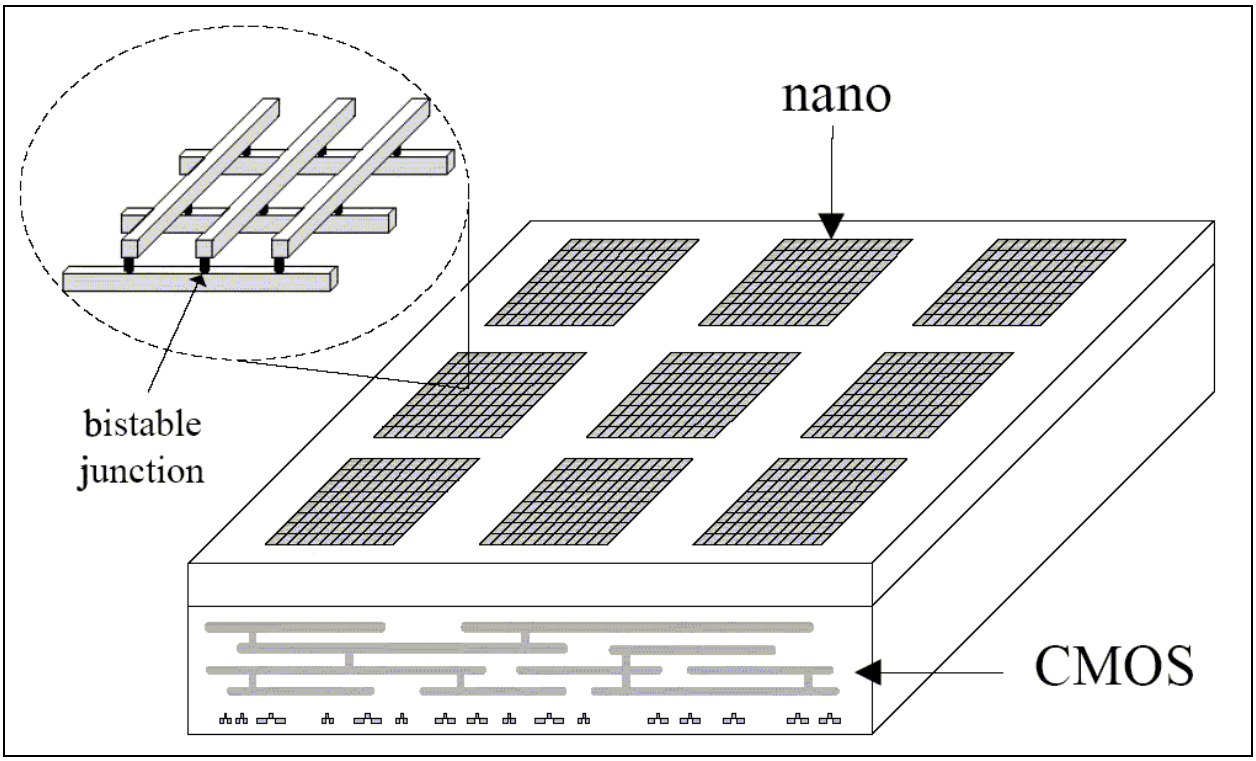

Figure 3. Nanoelectronics on a CMOS IC. (Zeigler &Stan, 2002)